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| 10/530,425 | 04/05/2005 | Kees Gerard Willem Goossens | NL03 0793 US | 6693 |

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| EXAMINER | |
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| DRABIK, SARAH E | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/530,425 | GOOSSENS, KEES GERARD WILLEM | |
| | Examiner | Art Unit | |
| | SARAH E. DRABIK | 2455 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 June 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 May 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This action is responsive to the Request for Continued Examination filed on June 17, 2009. Claims 1-2, 6-8, and 14-16 were amended. In response to amendments and clarifications made by the Applicant, the previous objections to the drawings are withdrawn.

Claims 1-16 are currently pending.

### *Claim Objections*

2. Claim 1 is objected to because of the following informalities: on line 22, "further determine" should be deleted. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

For claim 1, line 4, "one of said modules S" has no antecedent basis, but seems to refer back to the plurality of modules previously recited. If this is true, it is suggested to change "one of said modules S" to --one of said plurality of modules S--. On line 11, "said address translation means" has no antecedent basis, but seems to refer back to

the at least one address translation means previously recited. On line 17, "said translation unit" has no antecedent basis.

In claim 1, reference is made variously to an address translation means (presumably the same as the at least one address translation means first mentioned) and to a translation unit. However, the specification and claim 6 (the method counterpart to this claim) seem to indicate that these two components should be the same unit. If this is true, a single reference term should be chosen and consistently used throughout the claim and its dependent claims.

Also in claim 1, lines 8-10 recite: "at least one address translation means for receiving said message issued by said first module M comprising said first and second information and arranging the first and the second information as a single address". As the address translation means has already been disclosed as creating the single address, it seems that the limitations outlined on lines 12-18 are redundant. Additionally, lines 12-16 recite that the address translation means determines an addressed module S by examining the first or second information of the single address; however, the limitations of lines 19-24 inconsistently then recite that the addressed module S is determined simply based on the single address.

For claim 2, line 4, "said address translation means" has no antecedent basis, but seems to refer back to the at least one address translation means previously recited.

For claim 3, line 1, "said address translation means" has no antecedent basis, but seems to refer back to the at least one address translation means previously

recited. On line 2, "said interface means" has no antecedent basis, but seems to refer back to the network interface means previously recited. Also on line 2, "said first module" has no antecedent basis, but seems to refer back to the first module M previously recited.

For claim 4, line 1, "said address translation means" has no antecedent basis, but seems to refer back to the at least one address translation means previously recited. On line 3, it is unclear what global and local memory mapping is, and how it relates to the addressing scheme, particularly the first and second information and the address translation means, of the first claim.

For claim 6, line 4, "one of said modules S" has no antecedent basis, but seems to refer back to the plurality of modules previously recited. On lines 9, 11, and 13, "said translation unit" has no antecedent basis, but seems to refer back to the address translation unit previously recited.

For claim 7, "said master and addressed modules" has no antecedent basis. There is no master module disclosed (though there is a first module M), and there is only a single addressed module (S).

For claim 14, line 1, "one of said modules" has no antecedent basis, but seems to refer back to the plurality of modules, and the one module S, previously recited.

For claim 15, line 1, "said at least one network interface means" has no antecedent basis, but seems to refer back to the network interface previously recited. On line 3, "said at least one network interface" also has no antecedent basis, but seems to refer back to the network interface previously recited.

Claims 5 and 8-13 are rejected as being dependent on a rejected claim.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-4, 6-8, 10, and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Feyerabend (EP 1,083,768) in view of Applicant's Admitted Prior Art (AAPA).

Feyerabend discloses the invention substantially as claimed, including a system and method whereby a subscriber identity can be determined according to a first and second portion of an IP address (Feyerabend, Abstract).

For claim 1, Feyerabend discloses at least one address translation means for receiving the message issued by the first module M comprising the first and second

information and arranging the first and the second information as a single address (see, for example, col. 8, lines 32-34; col. 13, lines 9-18; and Fig. 6, where the first module M is the host 110, the addressed module S is the subscriber station 180, and the at least one address translation means is the address conversion unit 140),

wherein the address translation means is adapted to:

determine which module S is being addressed in the received message based on the first information of the single address (see, for example, col. 13, lines 30-35, and col. 14, lines 18-20);

arranging, at the translation unit, the first and the second information comprising the message as a single address (see col. 8, lines 32-34; col. 13, lines 9-18; and Fig. 6); and

determining, at a translation unit, which addressed module S is being addressed in the message issued from the first module M based on the single address (see col. 13, lines 30-35, and col. 14, lines 18-20).

However, Feyerabend does not disclose an integrated circuit comprising a plurality of modules and a network arranged for transferring messages between the modules wherein a message issued by a first module M comprises first information indicative of a location of one of the modules S being addressed within the network, and second information indicative of a particular location within the addressed module S, such as a memory or a register address. But the AAPA does disclose these limitations, including the following:

an integrated circuit comprising a plurality of modules and a network arranged for transferring messages between the modules (see pg. 1, lines 7-20), wherein a message issued by a first module M comprises first information indicative of a location of one of the modules S being addressed within the network, and second information indicative of a particular location within the addressed module S, such as a memory or a register address (see pg. 4, lines 3-6).

Additionally, in Feyerabend, the disclosed second information of the single address is used to further determine more precisely the location of the subscriber terminal (the module S) within a network, both before and after the creation of the single address. However, using the second information of the AAPA (the second information indicative of a particular location within the addressed module S) would result in that location information being encoded in the new single address, thus leading the address translation means to further determine the particular location within the addressed module S based on the second information of the single address and based on the single address.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have used the address translator of Feyerabend in the on-chip network disclosed by the AAPA, the motivation for doing so being to more accurately and efficiently determine where to route a message without the cost of maintaining plural lookup tables.

For claim 2, the combination of Feyerabend and AAPA discloses all subject matter of the claimed invention as discussed above with respect to claim 1.

Additionally, Feyerabend further discloses at least one network interface means associated to one of the modules for managing communication between one of the associated modules and the network, wherein one of the address translation means is arranged in one of the interface means (see, for example, col. 8, lines 22-31, and col. 9, lines 13-15, where the network interface means is the gateway 130).

For claim 3, the combination of Feyerabend and AAPA discloses all subject matter of the claimed invention as discussed above with respect to claim 2. Additionally, Feyerabend further discloses that the address translation means is arranged in the interface means associated to the first module (see col. 8, lines 22-31; col. 9, lines 13-15; and col. 10, lines 21-23).

For claim 4, the combination of Feyerabend and AAPA discloses all subject matter of the claimed invention as discussed above with respect to claim 2. Additionally, Feyerabend further discloses that the address translation means comprises an address mapping table configured to store relations between global and local memory mapping (see, for example, col. 13, lines 30-35 and lines 46-51; col. 14, lines 18-20; and Fig. 6).

For claim 6, Feyerabend discloses a method comprising the following:
the first module M issuing a message to an address translation unit (see col. 8, lines 23-25; col. 9, lines 13-15; and col. 10, lines 21-23, where the first module M is the host 110 and the address translation unit is the address conversion unit 140);

arranging, at the translation unit, the first and the second information comprising the message as a single address (see, for example, col. 8, lines 32-34; col. 13, lines 9-18; and Fig. 6); and

determining, at the translation unit, which module S is being addressed in the message issued from the first module M based on the single address (see col. 14, lines 18-53).

However, Feyerabend does not disclose an integrated circuit comprising a plurality of modules, the messages between the modules being exchanged via a network, wherein a message issued by a first module M comprises first information indicative of a location of one of the modules S being addressed within the network, and second information indicative of a particular location within the addressed module S, such as a memory or a register address. But the AAPA does disclose these limitations, including the following:

an integrated circuit comprising a plurality of modules, the messages between the modules being exchanged via a network (see pg. 1, lines 7-20),

wherein a message issued by a first module M comprises first information indicative of a location of one of the modules S being addressed within the network, and second information indicative of a particular location within the addressed module S, such as a memory or a register address (see pg. 4, lines 3-6).

Additionally, in Feyerabend, the disclosed second information of the single address is used to further determine more precisely the location of the subscriber terminal (the module S) within a network, both before and after the creation of the single address. However, using the second information of the AAPA (the second information

indicative of a particular location within the addressed module S) would result in that location information being encoded in the new single address, thus leading the address translation unit to further determine, at the translation unit, the particular location within the addressed module S based on the single address.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have used the address translator of Feyerabend in the on-chip network disclosed by the AAPA, the motivation for doing so being to more accurately and efficiently determine where to route a message without the cost of maintaining plural lookup tables.

For claim 7, the combination of Feyerabend and AAPA discloses all subject matter of the claimed invention as discussed above with respect to claim 6. Additionally, Feyerabend further discloses that a network interface is associated with one of the master and addressed modules (see, for example, col. 8, lines 22-31, where the network interface is the gateway 130).

For claim 8, the combination of Feyerabend and AAPA discloses all subject matter of the claimed invention as discussed above with respect to claim 6. Additionally, Feyerabend further discloses that communication between the plurality of modules is performed over connections (see Fig. 1).

For claim 10, the combination of Feyerabend and AAPA discloses all subject matter of the claimed invention as discussed above with respect to claim 8. Additionally, Feyerabend further discloses that connection types comprise simple

connections, multicast connections, narrowcast connections (see, for example, Fig. 1, the connections between the various components).

For claim 12, the combination of Feyerabend and AAPA discloses all subject matter of the claimed invention as discussed above with respect to claim 10. Additionally, Feyerabend further discloses that the simple connection is a connection between a message sending module and a single addressed module (see, for example, Fig. 1, the connection between gateway 130 and subscriber record database 150).

For claim 13, the combination of Feyerabend and AAPA discloses all subject matter of the claimed invention as discussed above with respect to claim 10. Additionally, Feyerabend further discloses that the multicast and narrowcast connections are connections between a message sending module and one or more addressed modules (see, for example, col. 6, lines 2-8, and Fig. 1, the connection between host 110 and network 120, within which a number of subscriber stations similar to subscriber station 180 may commonly be found).

For claim 14, the combination of Feyerabend and AAPA discloses all subject matter of the claimed invention as discussed above with respect to claim 10. Additionally, Feyerabend further discloses that the one of the modules being addressed has an address comprised of a global and a local address (see, for example, col. 13, lines 30-37 and lines 46-49).

For claim 15, the combination of Feyerabend and AAPA discloses all subject matter of the claimed invention as discussed above with respect to claim 7. Additionally, Feyerabend further discloses that the at least one network interface means

comprises at least two network interface ports to allow a module associated with the at least one network interface to communicate with a router network or at least one other module from among the plurality of modules (see Fig. 1, the plural connections from gateway 130).

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Feyerabend in view of AAPA as applied to claim 4 above, and further in view of Pham (US 6,446,173).

Feyerabend discloses the invention substantially as claimed, including a system and method whereby a subscriber identity can be determined according to a first and second portion of an IP address (Feyerabend, Abstract).

For claim 5, the combination of Feyerabend and AAPA discloses all subject matter of the claimed invention as discussed above with respect to claim 4, with the exception of the address mapping table containing specifically fields for every channel of a connection, for network interface ports of a connection, and for local addresses in addressed modules. However, Pham from the same or similar field of endeavor does disclose this limitation (see, for example, col. 5, lines 15-24; col. 9, lines 11-20; Fig. 1, components 21-28; and Fig. 3, components 204 and 104-112). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have used the specific mapping table fields disclosed by Pham in the address mapping tables of Feyerabend and AAPA, the motivation for doing so being to provide more complete information about a given module.

9. Claims 9, 11, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Feyerabend in view of AAPA as applied to claims 2 and 8 above, and further in view of Sgroi et al. ("Addressing the System-on-a-Chip Interconnect Woes Through Communication-Based Design").

Feyerabend discloses the invention substantially as claimed, including a system and method whereby a subscriber identity can be determined according to a first and second portion of an IP address (Feyerabend, Abstract).

For claim 9, the combination of Feyerabend and AAPA discloses all subject matter of the claimed invention as discussed above with respect to claim 8, with the exception of a connection comprising specifically a set of channels, each channel having a set of connection properties between a first module and at least one second module. However, Sgroi et al. from the same or similar field of endeavor do disclose this limitation (see, for example, Section 3.1, sixth paragraph). Thus, it would have been obvious to one of ordinary skill in the art at the time of the endeavor to have used the channels described by Sgroi et al. in the integrated circuit network of Feyerabend and AAPA, since such channels are necessary to physically implement the required connections.

For claim 11, the combination of Feyerabend and AAPA discloses all subject matter of the claimed invention as discussed above with respect to claim 9. Additionally, Sgroi et al. further teach that connection properties comprise ordering, flow control, throughput, latency, lossiness, transmission termination, transaction completion,

data correctness, priority, and data delivery (see, for example, Section 3.1, sixth paragraph). Thus, it would have been obvious to one of ordinary skill in the art at the time of the endeavor to have used the specific connection properties described by Sgroi et al. in the integrated circuit network of Feyerabend and AAPA, the motivation for doing so being to optimize inter-modular communication.

For claim 16, the combination of Feyerabend and AAPA discloses all subject matter of the claimed invention as discussed above with respect to claim 2, with the exception of the network interface means being configured specifically to send read and write requests and operations between at least one other network interface over the network. However, Sgroi et al. from the same or similar field of endeavor do disclose this limitation (see, for example, Section 3.1, sixth paragraph). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have allowed the specific read and write requests described by Sgroi et al. to be communicated in the integrated circuit network of Feyerabend and AAPA, the motivation for doing so being to allow a module to complete a given task or calculation.

### *Response to Arguments*

10. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SARAH E. DRABIK whose telephone number is (571)270-3990. The examiner can normally be reached on Monday through Friday, 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Najjar Saleh can be reached on 571-272-4006. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. E. D./
Examiner, Art Unit 2455
7/10/2009
/saleh najjar/

Supervisory Patent Examiner, Art Unit 2455